

**STATEMENT UNDER 37 CFR 3.73(b)**Applicant/Patent Owner: Denali Software, Inc.Application No./Patent No.: 10/663,328 Filed/Issue Date: September 16, 2003Titled: Method and Apparatus for Multi-Port Memory Controller

Cadence Design Systems, Inc., a corporation  
 (Name of Assignee) (Type of Assignee: corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in  
 (The extent (by percentage) of its ownership interest is \_\_\_\_\_ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

OR

- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Denali Software, Inc. To: Cadence Design Systems, Inc.

The document was recorded in the United States Patent and Trademark Office at  
 Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

2. From: SHRADER, Steven, et. al. To: Denali Software, Inc.

The document was recorded in the United States Patent and Trademark Office at  
 Reel 015015, Frame 0823, or for which a copy thereof is attached.

3. From: \_\_\_\_\_ To: \_\_\_\_\_

The document was recorded in the United States Patent and Trademark Office at  
 Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet (s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Thomas D. Franklin/  
 Signature

April 1, 2011  
 Date

Thomas D. Franklin, Reg. No. 43,616  
 Printed or Typed Name

Attorney  
 Title

## PATENT ASSIGNMENT

This Patent Assignment (the "**Assignment**") is made and effective as of March 28, 2011 (the "**Effective Date**"), by and between Denali Software, Inc., a California corporation (the "**Assignor**"), and Cadence Design Systems, Inc., a Delaware corporation (the "**Assignee**").

WHEREAS, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all of Assignor's right, title and interest, if any, in all patented and patentable ideas, including the patents, patent applications and invention disclosures that are identified in the *Schedule* to this Assignment attached hereto (the "**Assigned Patents**"). All capitalized terms used and not otherwise defined in this Assignment shall have the respective meanings set forth in the Asset Purchase Agreement.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Assignor hereby agrees as follows:

1. Assignment. To the extent Assignor has any rights, title or interest, Assignor hereby irrevocably and without reservation:

1.1 assigns to Assignee all of Assignor's right, title and interest whatsoever, throughout the world, in, to and under the Assigned Patents (including any patents that issue on the patent application included in the Assigned Patents or that issue from or are based upon continuations, continuations-in-art, divisions, reissues or extensions of the Assigned Patents), to have and to hold the same, unto Assignee, its successors and/or assigns, for the full duration of all such rights, and any renewals and extensions thereof;

1.2 transfers, conveys and assigns unto Assignee the entire right, title and interest in and to any and all causes of action and rights of recovery for past infringement of the Assigned Patents; and

1.3 agrees to execute and deliver such other documents and to take all such other actions, without any further consideration, that the Assignee, its successors and/or assigns may reasonably request to effect the terms of this Assignment, and to execute and deliver any and all affidavits, testimonies, declarations, oaths, samples, exhibits, specimens and other documentations as may be reasonably required to effect the terms of this Assignment and its recordation in all relevant Patent offices.

2. Governing Law. This Assignment shall be governed by and construed in accordance with the laws of the State of California without regard to its principles of conflicts of law. If any provision of this Assignment is held by a court of competent jurisdiction to be unenforceable, then such provision shall be eliminated or limited to the extent required by applicable law and this Assignment, as so modified, shall remain enforceable in accordance with its terms.

4. Waiver; Amendments. Any failure to enforce any provision of the Assignment shall not constitute a waiver thereof or of any other provision. This Assignment may not be amended, nor any obligation waived, except by a writing signed by both parties; nor shall any


NOT FOR RECORDATION

obligation herein be waived except in a writing signed by the person charged with making such waiver.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be duly executed and delivered as of the Effective Date.

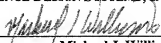
**ASSIGNOR:**

**DENALI SOFTWARE, INC.**

By:   
Name: Sharon Segev  
Title: Assistant Secretary

**ASSIGNEE:**

**CADENCE DESIGN SYSTEMS, INC.**

By:   
Name: Michael J. Williams  
Title: VP & Associate General Counsel

*Schedule to the Patent Assignment*

Docket No.	Title	App. No.	Date Filed	Pat. No.	Issue Date
DENAP001	Method and Apparatus for Multi-Port Memory Controller	10/663,328	9/16/2003	7,054,968	5/30/2006
DENAP002	Port Independent Data Transaction Interface for Multi-Port Devices	10/663,327	9/16/2003	7,100,002	8/29/2006
DENAP003	Reactive Placement Controller For Interfacing With Banked Memory Storage	10/702,916	11/5/2003	7,299,324	11/20/2007
DENAP003A	Reactive Placement Controller For Interfacing With Banked Memory	11/869,692	10/9/2007	7,574,573	8/11/2009
DENAP003B	Reactive Placement Controller For Interfacing With Banked Memory Storage	12/534,004	7/31/2009		
DENAP004	System and Method for Building Configurable Designs With Hardware Description and Verification Languages	11/752,141	5/22/2007	7,886,251	2/08/2011
DENAP005	System and Method for Providing Copyback Data Integrity in a Non-Volatile Memory System	11/778,433	7/16/2007		
DENAP006	System and Method for Providing Copyback Data Integrity in a Non-Volatile Memory System	12/022,134	1/29/2008		
DENAP007.PCT	System and Method for Wear Leveling Utilizing a Relative Wear Counter	PCT/US08/77863	9/26/2008	NA	NA
DENAP007	System and Method for Wear Leveling Utilizing a Relative Wear Counter	11/938,725	11/12/2007	7,876,616	1/25/2011
DENAP008+	Delay Compensation Circuit for Capturing and Sending DDR Memory Device Data	60/322,538	9/14/2001	NA	NA
DENAP008	Input/Output Cells For a Double Data Rate (DDR) Memory Controller	10/210,858	7/31/2002	7,062,625	6/13/2006
DENAP009	Programmable Delay Compensation Circuit	10/211,691	7/31/2002	6,665,230	12/16/2003
DENAP010	Method and Apparatus for Memory Management in a Non-Volatile Memory System Using a Block Table	12/022,138	1/29/2008		
DENAP011	Read Disturbance Management in a Non-Volatile Memory System	12/022,146	1/29/2008		
DENAP012	Method and Apparatus for Dynamically Configurable Multi Level Error Correction	12/143,274	6/20/2008		
DENAP013	Method and Apparatus for Parallel ECC Error Location	12/170,237	7/9/2008		
DENAP014	Method and Apparatus for High Speed Cache Flushing in a Non-Volatile Memory	12/040,782	2/29/2008		

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Docket No.	Title	App. No.	Date Filed	Pat. No.	Issue Date
DENAP015	System and Method for Managing Non-Volatile Memory Based on Health	12/201,937	8/29/2008		
DENAP016	Double Data Rate Memory Physical Interface High Speed Testing Using Self Checking Loopback	12/413,928	3/30/2009		
DENAP017	Method and Apparatus for Improving Small Write Performance in a Non-Volatile Memory	12/248,690	10/9/2008		
DENAP018	Method and Apparatus for Gate Training in Memory Interfaces	12/413,998	3/30/2009		
DENAP019	Method and Apparatus for Determining Write Leveling Delay for Memory Interfaces	12/414,044	3/30/2009		
DENAP020	Method and Apparatus for Transferring Data Between Asynchronous Clock Domains	12/435,550	5/5/2009		
DEN-P001US	Configurable and Reusable NAND System	11/934,790	11/5/2007		
DEN-P002	Execute-In-Place Implementation for a NAND Device	11/840,217	8/17/2007		
DEN-P003	Programmable Sequence Generator for a Flash Memory Controller	11/856,063	9/17/2007		
DEN-P004	Operation Based Polling in a Memory System	12/054,391	03/25/2008		
DENAP021	System and Method for Providing Copyback Data Integrity Using error Checking Logic				
DENAP022	System and Method for Non-Volatile Memory Page Management Using a Block Table Supporting Page Information				
DENAP023	Method and Apparatus for Solid State Drive Longevity Using A Recovery Memory Page				
DENAP024	Digital Oversampling Pattern Matching for Read Capture of Memory Data				
DEN004166	Programmable NAND Flash Controller for SoC Integration				
DEN004888	Striping of ECC data in Nand Flash				
DEN004889	Skipping of bad block sector in a page in Flash Nand				
DEN005204	Raid Implementation in HW Proposal				
DEN005205	RAID Implementation Attachment A				

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Docket No.	Title	App. No.	Date Filed	Pat. No.	Issue Date
DEN005206	RAID Implementation Attachment B				
DEN005304	Dual DDR2-DDR3 ODT for a single memory controller				
DEN005620	Rate-adaptive clock-agnostic asynchronous interface design				
DEN005621	Multiport Locking Method				
DEN006655	A hardware address restructuring method to accomplish multi-plane device accesses without any change in software.				
DEN006656	An Operation based priority interleaving method to increase the effective bandwidth of a system				
DEN006657	A software assisted hardware programming method to work with a wide variety of non-volatile memory devices efficiently				
DEN007816	Digital oversampling pattern matching for read capture of DDR SDRAM data				
DEN007817	Support Page Digital oversampling pattern matching for read capture of DDR SDRAM data				
DEN007818	RAID for SSD longevity				
DEN007819	Support Page RAID for SSD longevity				